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What is claimed is:

1 1. A method for manufacturing a capacitor of a semiconductor device,  
2 comprising:  
3 forming a storage electrode over a semiconductor substrate;  
4 forming a high dielectric layer over the storage electrode;  
5 forming a plate electrode over the high dielectric layer;  
6 performing a first post-annealing of the semiconductor substrate under an inert  
7 atmosphere at a first temperature; and  
8 performing a second post-annealing of the semiconductor substrate, after the first  
9 post-annealing, at a second temperature lower than the first temperature.

10 2. A method for manufacturing a capacitor of a semiconductor device, as recited  
11 in claim 1, wherein the high dielectric layer comprises a material selected from the group  
12 consisting of (Sr, Ti)O<sub>3</sub>, (Ba, Sr)TiO<sub>3</sub>, Pb(Zr, Ti)O<sub>3</sub>, and (Pb, La)(ZrTi)O<sub>3</sub>.

13 3. A method for manufacturing a capacitor of a semiconductor device, as recited  
14 in claim 1, wherein the plate electrode and the storage electrode comprises a material  
15 selected from the group consisting of Pt, Ru, Ir, IrO<sub>2</sub>, RuO<sub>2</sub>, SrRuO<sub>3</sub>, CaSrRuO<sub>3</sub>,  
16 BaSrRuO<sub>3</sub>, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

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1 4. A method for manufacturing a capacitor of a semiconductor device, as recited  
2 in claim 1, wherein the first temperature is between 600°C and 900°C.

1 5. A method for manufacturing a capacitor of a semiconductor device, as recited  
2 in claim 1, wherein the second temperature is between 100°C and 600°C.

1 6. A method for manufacturing a capacitor of a semiconductor device, as recited  
2 in claim 1, wherein the first and second post-annealing steps are performed separately or  
in-situ.

7. A method for manufacturing a capacitor of a semiconductor device, as recited  
in claim 1, wherein the first and second post-annealing steps are performed in a furnace or  
a rapid vacuum thermal annealing apparatus.

8. A method for manufacturing a capacitor of a semiconductor device, as recited  
2 in claim 1, wherein the first and second post-annealing steps are performed after the step  
3 of forming the high dielectric layer.

4 9. A method for manufacturing a capacitor of a semiconductor device, as recited  
in claim 1, wherein the first and second post-annealing steps are performed after the step  
of forming the plate electrode.

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1           10. A method for manufacturing a capacitor of a semiconductor device, as recited  
2   in claim 1, wherein the first post-annealing step is performed after the step of forming the  
3   high dielectric layer and the second post-annealing step is performed after the step of  
4   forming the plate electrode.

1           11. A method for manufacturing a capacitor of a semiconductor device, as recited  
2   in claim 1, further comprising forming an interdielectric layer over the plate electrode.

12. A method for manufacturing a capacitor of a semiconductor device, as recited  
in claim 11, wherein the first and second post-annealing steps are performed after the step  
of forming the interdielectric layer.

13. A method for manufacturing a capacitor of a semiconductor device, as recited  
in claim 11, wherein the first post-annealing step is performed after the step of forming  
the high dielectric layer and the second post-annealing step is performed after the step of  
forming the plate electrode.

1           14. A method for manufacturing a capacitor of a semiconductor device, as recited  
2   in claim 1, further comprising performing a third post-annealing, after the second post-  
3   annealing, at a third temperature lower than the second temperature.

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1 15. A method for manufacturing a capacitor of a semiconductor device in which a  
2 storage electrode, a high dielectric layer, a plate electrode, and an interdielectric layer are  
3 sequentially formed on a semiconductor substrate, further comprising:

4 performing a first post-annealing of the semiconductor substrate under an inert  
5 atmosphere at a first temperature, after forming one of the high dielectric layer, the plate  
6 electrode, and the interdielectric layer; and

7 performing a second post-annealing of the semiconductor substrate, after the first  
8 post-annealing, at a second temperature lower than the first temperature.

16. A method for manufacturing a capacitor of a semiconductor device, as recited  
in claim 15, wherein the high dielectric layer comprises a material selected from the  
group consisting of (Sr, Ti)O<sub>3</sub>, (Ba, Sr)TiO<sub>3</sub>, Pb(Zr, Ti)O<sub>3</sub>, and (Pb, La)(ZrTi)O<sub>3</sub>.

17. A method for manufacturing a capacitor of a semiconductor device, as recited  
in claim 15, wherein the plate electrode and the storage electrode comprise a material  
selected from the group consisting of Pt, Ru, Ir, IrO<sub>2</sub>, RuO<sub>2</sub>, SrRuO<sub>3</sub>, CaSrRuO<sub>3</sub>,  
BaSrRuO<sub>3</sub>, an alloy containing Pt, an alloy containing Ru, and an alloy containing Ir.

18. A method for manufacturing a capacitor of a semiconductor device, as recited  
in claim 15, wherein the first temperature is between 600°C and 900°C.

